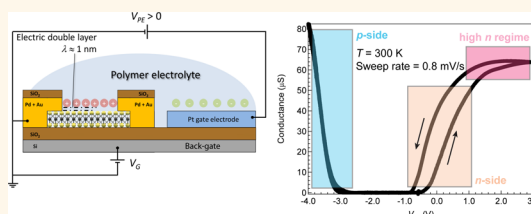


Electron and Hole Mobilities in Single-Layer WSe₂

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ABSTRACT Single-layer transition metal dichalcogenide WSe₂ has recently attracted a lot of attention because it is a 2D semiconductor with a direct band gap. Due to low doping levels, it is intrinsic and shows ambipolar transport. This opens up the possibility to realize devices with the Fermi level located in the valence band, where the spin/valley coupling is strong and leads to new and interesting physics. As a consequence of its intrinsically low doping, large Schottky barriers form between WSe₂ and metal contacts, which impede the injection of charges at low temperatures. Here, we report on the study of single-layer WSe₂ transistors with a polymer electrolyte gate (PEO:LiClO₄). Polymer electrolytes allow the charge carrier densities to be modulated to very high values, allowing the observation of both the electron- and the hole-doped regimes. Moreover, our ohmic contacts formed at low temperatures allow us to study the temperature dependence of electron and hole mobilities. At high electron densities, a re-entrant insulating regime is also observed, a feature which is absent at high hole densities.



KEYWORDS: tungsten diselenide · transition metal dichalcogenides · two-dimensional electronics · layered semiconductor · contacts · mobility

Semiconducting transition metal dichalcogenides (TMDs) have recently emerged as promising materials for electronics¹ and optoelectronics,^{2–5} exhibiting high charge carrier mobilities⁶ and mechanical robustness.⁷ These materials are particularly interesting in their monolayer form, where they exhibit a direct band gap and a broken inversion symmetry, which results in a coupled spin and valley degree of freedom.^{8–10} So far, MoS₂ has been the most widely studied TMD, due to its natural abundance. MoS₂ appears to be naturally n-doped, which has the advantage of allowing easy injection of charge carriers into the conduction band but makes it difficult to achieve p-type transport, which up to now was only observed in thicker samples.¹¹ On the other hand, monolayer WSe₂ has already been shown to exhibit ambipolar behavior,^{12–14} however, at the cost of difficulties in realizing good electrical contacts. Reaching the valence band is interesting from a technological standpoint, as it opens the possibility of designing planar p–n junctions,^{3–5} but it also holds promises for spintronics because large spin coherence time⁸ and electrical control of the spin¹⁵ have been predicted.

It is however difficult to engineer contacts to 2D semiconductors that perform

satisfactorily at low temperatures. The low-temperature transport of naturally n-doped MoS₂ has been difficult to study due to the non-ohmic nature of electrical contacts. Top-gated geometries⁶ or *in situ* annealing¹⁶ is required in order to achieve high carrier densities required for the electrodes to work properly. In intrinsic 2D semiconductors such as WS₂ and WSe₂, this problem is even more prominent. One possible solution is to chemically dope the contact area in order to induce very high carrier densities and produce ohmic behavior.^{12,14}

Here we report the study of single-layer WSe₂ transistors gated by the polymer electrolyte PEO:LiClO₄ (see Figure 1a). The superior electrostatic control offered by this ion gel allows very high carrier densities to be reached, and similar electrolytes have previously allowed the observation of ambipolar behavior in WS₂ at room temperature.^{17,18} Moreover, the atomic-scale thickness of the electric double layer (EDL) formed at the interface (see Figure 1b), which acts as a super-efficient capacitor, thins the Schottky barrier down to a regime where tunneling becomes the main charge injection mechanism.¹⁹ This allows efficient injection of both types of charge carriers, even at cryogenic temperatures, and to

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Received for review April 18, 2014 and accepted June 16, 2014.

Published online June 20, 2014
10.1021/nn5021538

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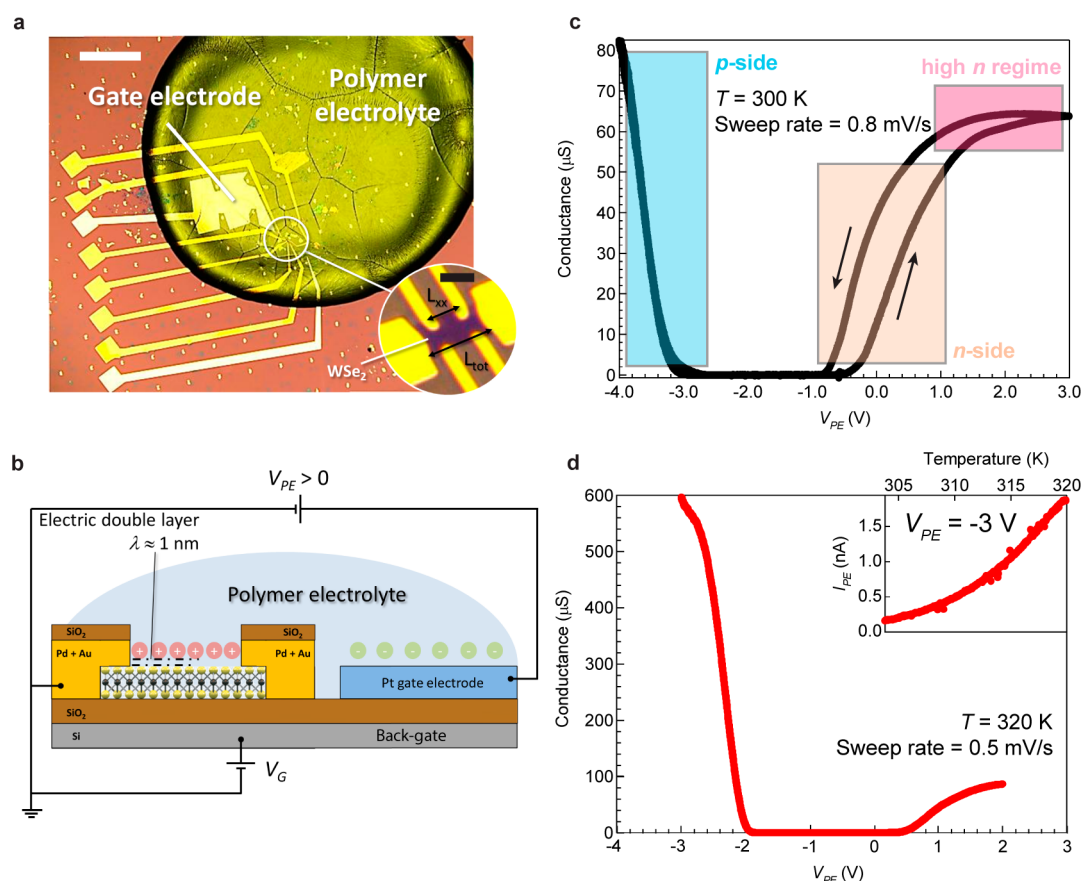


Figure 1. Polymer electrolyte-gated WSe₂ single-layer transistors. (a) Optical micrograph of the device. The scale bar is 500 μm . Inset: zoom on the transistor region. Scale bar is 3 μm . (b) Sketch of the charge configuration in the device for a positive voltage $V_{PE} > 0$ applied to the polymer electrolyte gate electrode; λ is the Debye length. (c) Room temperature ($T = 300\text{ K}$) transfer curve of the transistor. We can identify three regions of interest: hole-doped (hereafter referred to as “p-side”), slightly electron-doped (“n-side”), and highly electron-doped (“high n regime”). (d) High-temperature ($T = 320\text{ K}$) transfer curve of the same device. Inset: leakage current at $V_{PE} = -3\text{ V}$ as a function of temperature.

perform, for the first time, the study of the transport properties of single-layer WSe₂ as a function of temperature and both p- and n-type behavior on the same device. Figure 1a shows an optical micrograph of the finalized device. The device was annealed *in situ* at 80 °C in high vacuum prior to measurements.

RESULTS AND DISCUSSION

Figure 1c describes the behavior of the transistor at room temperature. When compared to ionic liquids, such as the widely used DEME-TFSI,^{20–22} PEO:LiClO₄ has a slower response but also superior mechanical stability at low temperatures and against repeated temperature cycling. The lower ionic conductivity of PEO:LiClO₄ is partially compensated by its large chemical stability window. At $T = 300\text{ K}$, polymer electrolyte gate voltages (V_{PE}) as low as $V_{PE} = -4\text{ V}$ can be applied with minimum leakage current $I_{\text{leak}} < 200\text{ pA}$. We can identify three regimes of interest (ROI) that we will focus on in the rest of this article: the hole transport regime (labeled “p-side”), the electron transport regime (“n-side”), and a regime at high electron density where the conductivity saturates (“high n regime”).

After the measurements as a function of temperature in these three regimes were completed, another transfer curve was acquired at a slightly higher temperature ($T = 320\text{ K}$; see Figure 1d). We can see that it results in significantly higher conductivities. A careful analysis also reveals that the apparent band gap is reduced. Similarly to previous observations when using DEME-TFSI on ZnO,²² we speculate that this effect is due to the higher carrier densities that can be accumulated at higher temperature for a given V_{PE} . For the low-temperature study, we proceeded in the following way: we apply a given value of V_{PE} for several hours at $T = 300\text{ K}$ and wait for the current to stabilize. In this way, we make sure that all the mobile ions in our gel had enough time to migrate to the EDL. This typically results in a substantial but reversible shift of the entire transfer curve, if acquired afterward (compare for example Figure 1c,d). The charge state of the sample could however be restored by baking it *in situ* to 80 °C for several hours, indicating that no permanent modification/degradation had occurred. We performed this charge “reset” before the study of each ROI in temperature. Finally, the ionic conductivity of PEO:LiClO₄

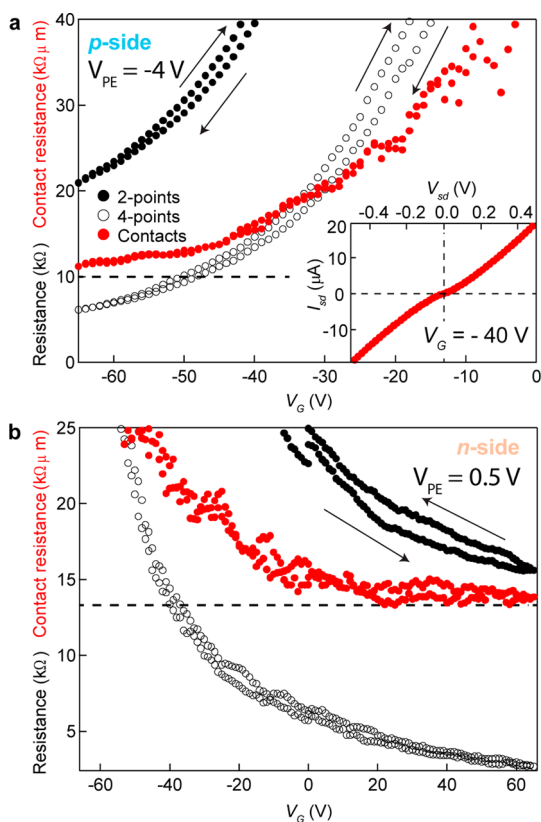


Figure 2. Contact resistance at low temperature ($T = 4$ K). Back-gate dependence of the two-point (filled black dots), four-point (open black dots), and contact resistance (red dots) (a) on the hole side and (b) on the electron side. The dotted line is a guide for the eye, representing the contact resistance achieved at high doping. The inset of (a) shows the $I(V)$ output curve recorded at $V_G = -40$ V.

rapidly drops as the temperature is lowered and the ions freeze around $T = 270$ K. In order to study the transport and field-effect mobility of the devices, we used the back-gate voltage V_G to modulate the charge carrier density below the freezing point. Our sample was remarkably stable below the freezing point, and the back-gate voltage or temperature history did not influence the measurements, as can be seen on Figure 2, where voltage traces and retraces are shown to exhibit very little hysteresis.

Figure 2 demonstrates that the use of the ion gel substantially decreases the contact resistance at cryogenic temperatures, thus allowing proper four-point measurements of the conductivity to be performed. Figure 2a (for the p-side) and Figure 2b (for the n-side) show the back-gate dependence at $T = 4$ K of the four-point resistance R_{4P} , two-point resistance R_{2P} , and the inferred contact resistance:

$$R_{\text{contacts}} = R_{2P} - \frac{L_{\text{tot}}}{L_{\text{xx}}} R_{4P}$$

where $L_{\text{tot}} = 5.3 \mu\text{m}$ and $L_{\text{xx}} = 2.4 \mu\text{m}$ are the total source-drain length and distance separating the voltage side probes, respectively (see Figure 1a). The contact

resistance decreases with increasing charge carrier concentration and seems to asymptotically approach a finite value, as indicated by the dashed lines. These values corresponds to $\rho_c \approx 10\text{--}13 \text{ k}\Omega \cdot \mu\text{m}$, a value which is lower than the best value recorded for single-layer MoS_2 transistors with solid top-gates.⁶ The output characteristic $I(V)$ is also nearly ohmic, as can be seen in the inset of Figure 2a.

Now that we have demonstrated that good electrical contacts have been realized, we can perform a temperature study of the four-point conductivity. Figure 3a (Figure 3b) shows the conductance as a function of back-gate voltage for different temperatures in the hole-doped (electron-doped) region. These two regimes show distinct behaviors. On the n-side, the behavior is very similar to previously studied electron transport in MoS_2 . The conductance increases with decreasing temperature, indicating a metallic behavior. We can measure the carrier density using the Hall effect (inset of Figure 3d) and calculate the field effect and Hall mobilities. The field-effect mobility, reported in Figure 3b for holes and Figure 3d for electrons, is given by

$$\mu_{\text{FE}} = \frac{1}{C_G} \frac{L_{\text{xx}}}{W} \frac{\partial G}{\partial V_G}$$

where $W = 2.9 \mu\text{m}$ and $L_{\text{xx}} = 2.4 \mu\text{m}$ are the width and the length of the device, G is the conductance, and $C_G = 1.39 \times 10^{-8} \text{ F} \cdot \text{m}^{-2}$ is the back-gate capacitance inferred from the Hall effect (see inset of Figure 3d). It starts at around $30 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at room temperature and reaches a value of $160 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at $T = 4$ K. The Hall mobility at $T = 4$ K (see Supporting Information Figure S1), which is proportional to the drift mobility of the electrons, is given by

$$\mu_{\text{Hall}} = \frac{\sigma}{en}$$

where σ is the conductivity, e the electron charge, and n the electron density extracted from the Hall effect measurements. Similarly to the case of MoS_2 ,¹⁶ it is dependent on the carrier density and asymptotically approaches the value of the field-effect mobility at high carrier densities. It reaches a value of $100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at $T = 4$ K for $n = 1.9 \times 10^{13} \text{ cm}^{-2}$. The p-side differs from the n-side in several respects: it is nonmetallic, has a higher and almost temperature-independent field-effect mobility, and the Hall effect could not be measured.

As shown on Figure 3a, the p-side displays values of conductance that are similar to those recorded on the n-side near room temperature. The temperature dependence is however different, with the conductivity slowly decreasing with decreasing temperature, thus displaying an insulating behavior. It seems that a metal–insulator transition can be extrapolated from the conductance curves in Figure 3c. Temperature scans performed at a later time and higher hole doping levels revealed that a metallic regime can indeed be reached

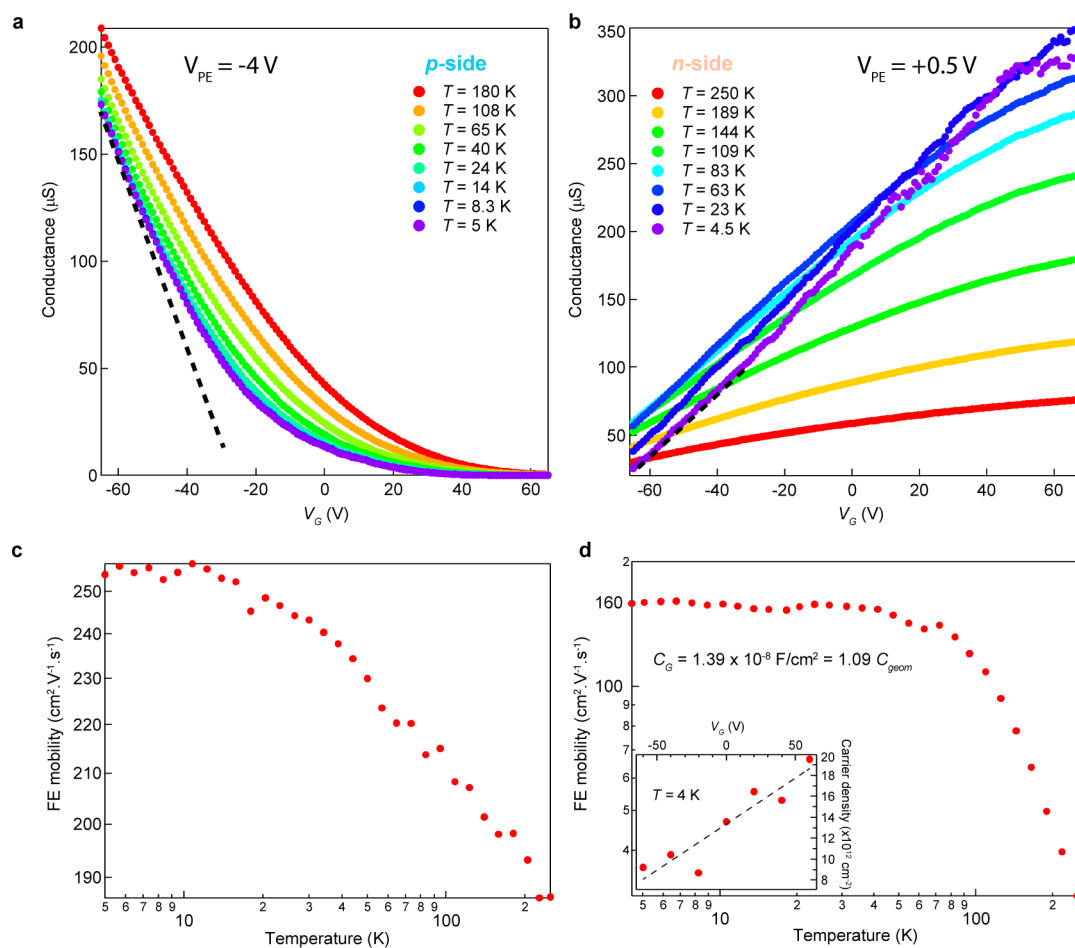


Figure 3. Electron and holes mobilities in single-layer WSe_2 . Conductance as a function of back-gate voltage at different temperatures on the (a) hole side and (b) electron side. The corresponding field-effect mobilities as a function of temperature, on the p-side (c) and n-side (d). In calculating the mobilities, we used the values of $\partial G/\partial V_G$ obtained in regions where the conductance displays a linear dependence on gate voltage (dashed lines in panels a and b). Inset of (d): carrier density on the n-side, measured using the Hall effect. The extracted back-gate capacitance is indicated.

on the p-side (see Figure S2), associated with perfectly ohmic (linear) $I(V)$ curves (see Figure S3). Contrary to the n-side and to previous results in MoS_2 ,⁶ the metal–insulator transition happens at a value of the sheet conductivity $\sigma \approx 7.5 e^2/h$, which is much higher than the value predicted by the Ioffe–Regel criterion.²³ Inhomogeneous current density (due to flake damage, for example) can be ruled out because the conductance measured from both sides of the flake is the same (see Figure S4). This could instead be due to a decrease in the density of thermally excited carriers with decreasing temperature or to a change of the band gap with temperature, all leading to a nonconstant carrier density at fixed back-gate voltage. This effect could be more pronounced on the p-side because the Fermi level naturally lies closer to the conduction band (see Figure 1c). The conductance nevertheless displays a linear regime, and the field-effect mobility for holes can be derived (see Figure 3c). It is systematically higher than the electron mobility, with a very weak temperature dependence. This indicates that the mobility is not yet phonon-limited and is limited by intrinsic sources

of scattering. The room temperature ($T = 250$ K) field-effect mobility of holes in WSe_2 ($180 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) is significantly higher than the best field-effect electron mobilities reported in MoS_2 ($60\text{--}100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) and consistent with previously reported values for WSe_2 (refs 12 and 13).

Compared to the hole mobility, the electron mobility starts to drop drastically above $T = 100$ K (see Figure 3d) and reaches $30 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at room temperature. This value is lower than previous reports of room temperature electron mobility in SL WSe_2 .^{13,14} We also notice that this mobility drop is concomitant with the onset of a sublinear regime in the conductance *versus* back-gate voltage. Looking back at Figure 1c, this might be the onset of the conductance saturation observed at high electron densities. Such saturation/decrease of the conductivity at high carrier densities (see Figure S5 for another example of the conductance drop at high positive V_{PE} at room temperature in another device) has been reported in bilayer and trilayer graphene and attributed to the onset of interband scattering.²¹ We know that the band structure of TMDs is affected

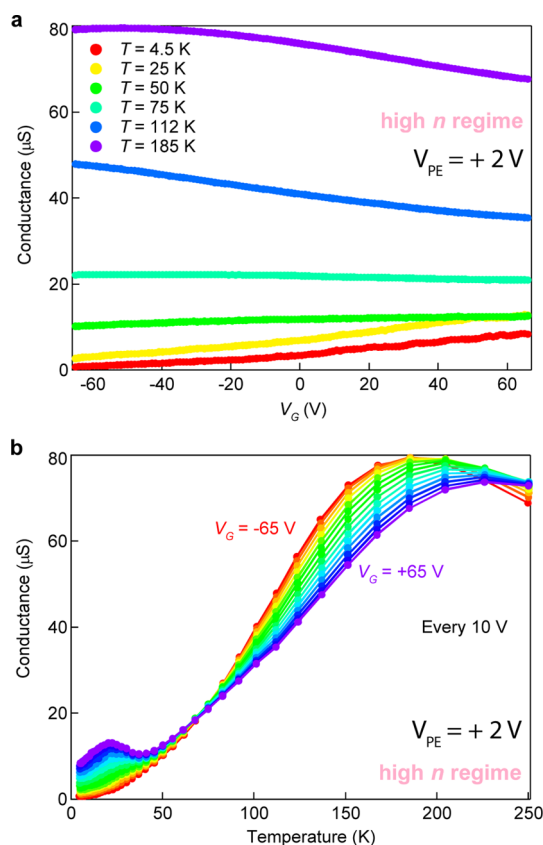


Figure 4. Insulating behavior in the highly electron-doped regime. (a) Conductance vs back-gate voltage at different temperatures. (b) Conductance vs temperature for different back-gate voltages.

by quantum confinement in the 2D limit.²⁴ Increased interband scattering could be one of the reasons why the mobility in single layers is systematically lower than that of bulk material.²⁵ Interestingly, the high-temperature dependence of the electron mobility in MoS₂ is very similar,⁶ which points to a similar scattering mechanism being at the origin of the mobility reduction.

METHODS

Device Fabrication. WSe₂ monolayer flakes were exfoliated onto Si/SiO₂ wafers and identified from their optical contrast.²⁶ Standard e-beam lithography and thermal evaporation were employed to create electrical contacts. These consist of 5 nm of Pd and 45 nm of Au and a capping layer of 15 nm of SiO₂ in order to isolate the metal contacts from the ionic gel. The gate electrode is made of 30 nm of Pt and was deposited during a separate evaporation. Its surface area is much larger than that of the WSe₂ flake, ensuring that most of the applied voltage drops at the surface of the WSe₂ flake, maximizing the gate efficiency. WSe₂ flakes were shaped into Hall bars with a well-defined channel geometry using oxygen plasma etching.

Electrolyte Preparation. The polymer electrolyte was prepared by dissolving an 8:1 mixture of polyethylene oxide (PEO) and lithium perchlorate (LiClO₄)²⁷ in acetonitrile to form a 10 wt % solution. The solution was sonicated and filtered using a syringe filter.²⁸ A droplet was deposited onto the device inside a glovebox (Ar atmosphere) and left to dry. The device had previously been degassed for 4 h at 100 °C in the glovebox to remove adsorbates.

Figure 4 shows the temperature and back-gate voltage dependence of the conductance, taken at high electron doping. Interestingly, the behavior is insulating, with a dependence on gate voltage that reverts as the temperature is decreased. This re-entrant insulating regime at high carrier densities is unexpected and not understood. It is not related to sample damage, as the behavior was fully reversible after warming up the sample.

CONCLUSION

In summary, we carried out the first study of the electron and hole transport in single-layer WSe₂ transistors as a function of temperature. The use of a polymer electrolyte gate allowed us to achieve ohmic contacts at cryogenic temperatures, which is a prerequisite for any electrical measurement. The temperature study of the electron-doped side reveals a behavior very similar to that of single-layer MoS₂, with a metallic state above $n = 8 \times 10^{12} \text{ cm}^{-2}$ and a strong suppression of the mobility at high temperatures. The hole-doped region shows a metal–insulator transition at much higher conductivity than expected from the Ioffe–Regel criterion. This speaks for a strong temperature dependence of the carrier density. The field-effect mobility is nearly temperature-independent, with a room temperature value which is consistent with previously reported values¹² and significantly higher than that of electrons. The regime with high levels of electron doping is surprisingly insulating. This work demonstrates for the first time that ohmic contacts can be formed with WSe₂ at low temperatures and is the first report of a temperature-dependent hole transport in a two-dimensional TMD. It thus paves the way for the realization of electrical devices taking advantage of the peculiar structure of the valence band of TMDs and to the demonstration of spin/valleytronic devices using these materials.

Conflict of Interest: The authors declare no competing financial interest.

Acknowledgment. The authors would like to thank D. Lembke for his help in preparing the ion gels, and T. Heine and A. Morpurgo for useful discussions. Device fabrication was carried out in part in the EPFL Center for Micro/Nanotechnology (CMI). We thank Z. Benes (CMI) for technical support with e-beam lithography.

Supporting Information Available: Hall mobility vs carrier density on n-side, metal–insulator transition on p-side, $I(V)$ output curve in the metallic regime on the p-side, transfer curves acquired from both sides of the flake on the p-side, $T = 320 K$ transfer curve in another device. This material is available free of charge via the Internet at <http://pubs.acs.org>.

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